CLAIMS

1. A ROM circuit (30, 40) including memory cell columns, each column being connected to a bit line (BL_i, BL_{i+1}), wherein the columns are arranged in groups of two adjacent columns (A_i, A_{i+1}), each column in a group being selectively activable or inactivable with respect to the other column in the group by means of an activation line (BS_i, BS_{i+1}), characterized in that each column in a group is connected by one end to the activation line (BS_i, BS_{i+1}) of the other column in the group.

2. The memory circuit of claim 1, wherein the activation line of a column is brought to the ground potential to deactivate said column.

3. The memory circuit of claim 1 or 2, wherein a column comprises a plurality of memory cells in series, each memory cell comprising a MOS transistor, the drain, respectively the source, of which is coupled either to the source, respectively the drain, of an adjacent memory cell, or to an end of the column.

4. The memory circuit of claim 3, wherein each column of a group comprises a selection means (35, 36) capable of selectively activating/deactivating said column, controlled by the activation line of the column.

5. The memory circuit of claim 4, wherein the selection means (BS_i, BS_{i+1}) of a column comprises a MOS transistor in series with the memory cells of the column and arranged at the end of the column not connected to the activation line of the other column of the group.

6. The memory circuit of any of claims 1-5, including an amplifier (41, 51) connected to the bit lines connected to the two columns of a same group.

7. The memory circuit of claim 6, wherein the amplifier (41, 51) includes a means for invalidating the information present on the bit line connected to the deactivated column in the group.

8. The memory circuit of claim 6, wherein the amplifier (41, 51) includes a means for lowering the voltage present on the bit line connected to the deactivated column in the group.